IN THE CLAIMS

Please amend the claims as set forth below in marked-up form:

1. (Original) A PLL circuit, comprising:

an oscillator for generating an oscillation frequency signal having a variable oscillation frequency;

a phase detection circuit for comparing the phases of the oscillation frequency signal of said oscillator and an input signal with each other and outputting, based on a result of the comparison, a first phase control signal for advancing the phase of the oscillation frequency signal of said oscillator or a second phase control signal for delaying the phase of the oscillation frequency signal of said oscillator;

a signal generation circuit for generating first and second signals having different phases from each other based on the oscillation frequency signal of said oscillator; and

a frequency detection circuit for fetching the first and second signals generated by said signal generation circuit in synchronism with the input signal for each period of the input signal, logically operating the fetched signals and signals having been fetched in the immediately preceding period and outputting, based on a result of the arithmetic operation, a first frequency control signal for raising the frequency of the oscillation frequency signal of said oscillator or a second frequency control signal for lowering the frequency of the oscillation frequency signal of said oscillator.

2. (Original) A PLL circuit according to claim 1, wherein the first and second signals are clock signals.

3. (Currently Amended) A PLL circuit according to claim 2, wherein the phases of the first and second signals ~~is different~~ differ from each other by 90 degrees ~~from each other~~.

4. (Original) A PLL circuit according to claim 1, wherein said frequency detection circuit includes a first sampling circuit for fetching the first signal in synchronism with the input signal for each period of the input signal, a second sampling circuit for fetching the second signal in synchronism with the input signal for each period of the input signal, and a control logic circuit for storing the signals fetched by said first and second sampling circuits, logically

operating the stored signals and the signals fetched subsequently by said first and second sampling circuits and generating, based on a result of the logical operation, the first frequency control signal or the second frequency control signal.

5. (Original) A PLL circuit according to claim 4, wherein said control logic circuit includes a first logical operation circuit for logically operating output signals of said first and second sampling circuits, a first storage circuit for storing an output signal of said first logical operation circuit, a second logical operation circuit for logically operating the output signals of said first and second sampling circuits and the stored signal of said first storage circuit, a third logical operation circuit for logically operating a signal obtained by logical processing of the output signals of said first and second sampling circuit and the stored signal of said first storage circuit, second storage means for storing an output signal of said second logical operation circuit, and third storage means for storing an output signal of said third logical operation circuit.

6. (Original) A PLL circuit according to claim 4, wherein said first and second sampling circuits sample the first and second signals, respectively, at a timing of a rising edge or a falling edge of the input signal.

7. (Original) A PLL circuit according to claim 4, wherein each of said first and second sampling circuits includes a flip-flop circuit.

8. (Original) A PLL circuit according to claim 7, wherein said flip-flop is a D-type flip-flop.

9. (Original) A PLL circuit according to claim 8, wherein the D-type flip-flops fetch the first and second signals at a timing of a rising edge of a clock input thereto.

10. (Original) A PLL circuit according to claim 5, wherein each of said first, second and third logical operation circuits includes an OR circuit.

11. (Original) A PLL circuit according to claim 5, wherein each of said first, second and third storage circuits includes a flip-flop circuit.

12. (Original) A PLL circuit according to claim 11, wherein said flip-flop circuit is a D-type flip-flop.

13. An optical communication reception apparatus, comprising:

light reception means for receiving an optical signal, converting the optical signal into an electric signal and outputting the electric signal;

a PLL circuit for producing a clock signal synchronized with the output signal of said light reception means; and

a retiming circuit for retiming the output signal of said light reception means based on the clock signal produced by said PLL circuit;

said PLL circuit including an oscillator for generating an oscillation frequency signal having a variable oscillation frequency, a phase detection circuit for comparing the phases of the oscillation frequency signal of said oscillator and an input signal with each other and outputting, based on a result of the comparison, a first phase control signal for advancing the phase of the oscillation frequency signal of said oscillator or a second phase control signal for delaying the phase of the oscillation frequency signal of said oscillator, a signal generation circuit for generating first and second signals having different phases from each other based on the oscillation frequency signal of said oscillator, and a frequency detection circuit for fetching the first and second signals generated by said signal generation circuit in synchronism with the input signal for each period of the input signal, logically operating the fetched signals and signals having been fetched in the immediately preceding period and outputting, based on a result of the arithmetic operation, a first frequency control signal for raising the frequency of the oscillation frequency signal of said oscillator or a second frequency control signal for lowering the frequency of the oscillation frequency signal of said oscillator.

14. (Original) An optical communication reception apparatus according to claim 13, wherein the first and second signals are clock signals.

15. (Currently Amended) An optical communication reception apparatus according to claim 14, wherein the phases of the first and second signals ~~is different~~differ from each other by 90 degrees ~~from each other~~.

16. (Original) An optical communication reception apparatus according to claim 13, wherein said frequency detection circuit includes a first sampling circuit for fetching the first signal in synchronism with the input signal for each period of the input signal, a second sampling circuit for fetching the second signal in synchronism with the input signal for each period of the input signal, and a control logic circuit for storing the signals fetched by said first and second sampling circuits, logically operating the stored signals and the signals fetched subsequently by said first and second sampling circuits and generating, based on a result of the logical operation, the first frequency control signal or the second frequency control signal.

17. (Original) An optical communication reception apparatus according to claim 16, wherein said control logic circuit includes a first logical operation circuit for logically operating output signals of said first and second sampling circuits, a first storage circuit for storing an output signal of said first logical operation circuit, a second logical operation circuit for logically operating the output signals of said first and second sampling circuits and the stored signal of said first storage circuit, a third logical operation circuit for logically operating a signal obtained by logical processing of the output signals of said first and second sampling circuit and the stored signal of said first storage circuit, second storage means for storing an output signal of said second logical operation circuit, and third storage means for storing an output signal of said third logical operation circuit.

18. (Original) An optical communication reception apparatus according to claim 16, wherein said first and second sampling circuits sample the first and second signals, respectively, at a timing of a rising edge or a falling edge of the input signal.